IDEC Chip Design Contest

A Framed Pulse Width Modulation Transceiver with Low Supply Voltage

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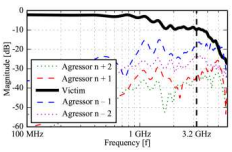
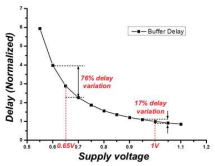
Background

• **Power is Cost**

• **Speed & Power Trade off**



<Channel Loss (DRAM)>

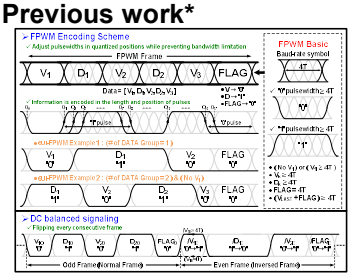


<Bandwidth vs. VDD>

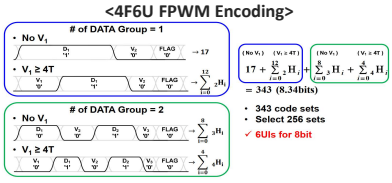
- More speed, more Power
- EQ needs additional Power
- Low VDD limits BW_{IC}

Framed Pulse Width Modulation

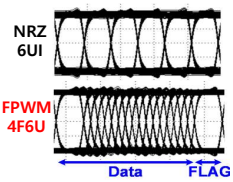
• **Previous work***



<4F6U FPWM Encoding>



<4F6U FPWM Data Sets >



<Eye Diagram of NRZ & FPWM>
(4F6U)

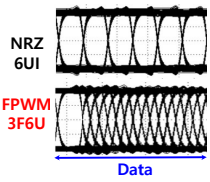
$$\text{Coding Gain} = \frac{8bit - 6UI}{6UI} \times 100\% = 33\%$$

- 33% more bits than NRZ
- LUT based Encoding
- TSMC 40nm CMOS

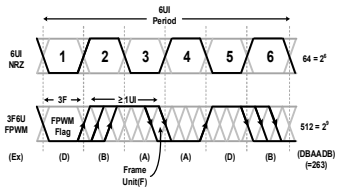
*: Ref, S. Jeon, et. al, ISSCC, 2018

Revised FPWM and Transceiver IC Architecture

• **Revised Encoding**



<Eye Diagram of NRZ & FPWM>
(3F6U)

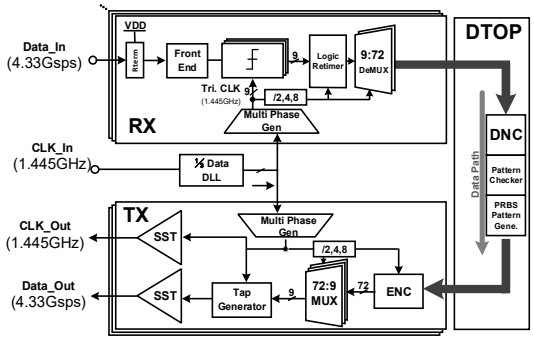


<3F6U FPWM Coding Scheme>

$$\text{Coding Gain} = \frac{9bit - 6UI}{6UI} \times 100\% = 50\%$$

- 50% more bits than NRZ
- $Data_{pre}$ Succesive Pattern based Encoder
- Samsung 65nm CMOS

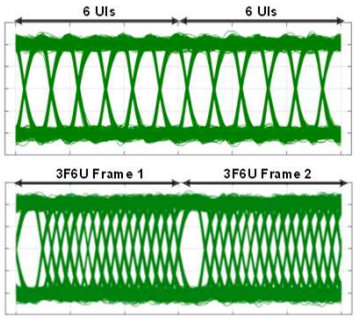
• **Top Architecture**



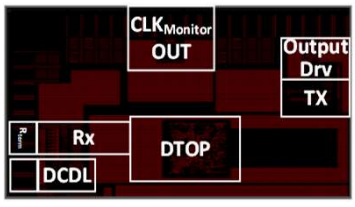
• **Features**

- Spectral Efficiency
  4.33GSps ➔ **6.5Gbps**
- Forwarded CLK & DLL
- PRBS based Encoder /Decoder & Checker
- Samsung 65nm CMOS

Area & Simulation



<Simulated Eye Diagram (4.33Gsps) >



Block	Area (um X um)	Block	Area (um X um)
Rx	460 X 350	CLK	460 X 96
Tx	450 X 740	DTOP	480 X 510

- Revision Issue : 9:1 Tx Mux
- DLL Loop

Test Result

Test Pattern Generation Result

<Baud rate 111_000 Pattern>

<Shortest Pattern 100_000>

- Revision Issue : 9:1 Tx Mux & Output Drv
  - Issue : Tx Mux CLK Path & Data path Bandwidth limitation
  - Must generate PRBS based Pattern

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